DATA PROCESSING SYSTEM USING MULTIPLE ADDRESSING MODES FOR SIMD OPERATIONS AND METHOD THEREOF

Related Applications

5   This is related to United States Application having attorney docket

10/657,570

number SC13053TH, filed on even date, and entitled "Data Processing

System Using Independent Memory And Register Operand Size Specifiers

And Method Thereof," United States Patent Application having attorney

10/657,331

10   docket number SC13074TH, filed on even date, and entitled "Data

Processing System Having Instruction Specifiers for SIMD Register

Operands and Method Thereof," United States Application having attorney

10/657,593, now US Patent 7,107,436

docket number SC13075TH, filed on even date, and entitled "Data

Processing System and Method of Providing Memory Operands for a SIMD

15   Processor," United States Application having attorney docket number

CML00107, 10/657,593, now US Patent 7,100,019

CML00104D, filed on even date, entitled "Partitioned Vector Processing,"

new US Patent 6,795,908

and application number 09/591,938, filed June 12, 2000, and entitled

"Method and Apparatus for Instruction Execution in a Data Processing

System", all of which are assigned to the current assignee hereof.

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Field of the Invention

The present invention relates generally to data processing systems, and

more specifically, to instructions for use within a data processing system.

25   ## Related Art

Increased performance in data processing systems can be achieved by

allowing parallel execution of operations on multiple elements of a vector.

One type of processor available today is a vector processor which utilizes